

GUANGYU HU



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Research Field

- Enhanced **Hardware Formal Verification** through the integration of advanced machine learning techniques.
- Implementation of Equality Saturation Framework for Efficient **Logic Synthesis**.
- AI for mathematics and formal reasoning (and vice versa), including **LLM-driven theorem proving** and **LLM reasoning verification**.

EDUCATION

Ph.D. in IIP (Microelectronics) | *Advisor: Hongce Zhang & Wei Zhang*

Feb. 2022 – 2025

 **The Hong Kong University of Science and Technology**

CGPA: 3.99/4.3 | Graduated

B.Eng. in Software Engineering (Honours)

Sep. 2016 – Feb. 2021

 **Xiamen University**

CGGPA: 3.41/4.0 | Ranked in the Top 20%

SELECTED PUBLICATION

(*Equal contribution, †Corresponding author.)

IC3-Evolve: Proof-/Witness-Gated Offline LLM-Driven Heuristic Evolution for IC3	2026
Mingkai Miao*, Guangyu Hu*, Ziyi Yang, Hongce Zhang	IJCAI
A-IC3: Learning-Guided Adaptive Inductive Generalization for Hardware Model Checking	2026
Xiaofeng Zhou*, Guangyu Hu*, Hongce Zhang, Wei Zhang	CAV
AutoPDR: Circuit-Aware Solver Configuration Prediction for Hardware Model Checking	2026
Guangyu Hu, Chen Chen, Xiaofeng Zhou, Jiaxi Zhang, Wei Zhang, Hongce Zhang	ISEDA
LeGenD: A Data-Driven Framework for Lemma Generation in Hardware Model Checking	2026
Mingkai Miao*, Guangyu Hu*, Wei Zhang, Hongce Zhang	DAC
EvolveGen: Algorithmic Level Hardware Model Checking Benchmark Generation through RL	2026
Guangyu Hu*, Xiaofeng Zhou*, Wei Zhang, Hongce Zhang	TACAS
BDD2Seq: Enabling Scalable Reversible-Circuit Synthesis via Graph-to-Sequence Learning	2026
Mingkai Miao, Jianheng Tang, Guangyu Hu†, Hongce Zhang	AAAI
E-morphic: Scalable Equality Saturation for Structural Exploration in Logic Synthesis	2025
Chen Chen*, Guangyu Hu*†, Cunxi Yu, Yuzhe Ma, Hongce Zhang	DAC
E-Syn: E-Graph Rewriting with Technology-Aware Cost Functions for Logic Synthesis	2024
Chen Chen*, Guangyu Hu*, Dongsheng Zuo, Cunxi Yu, Yuzhe Ma, Hongce Zhang	DAC
DeepIC3: Guiding IC3 Algorithms by Graph Neural Network Clause Prediction	2024
Guangyu Hu, Jianheng Tang, Changyuan Yu, Wei Zhang, Hongce Zhang	ASP-DAC
NeuroPDR: Integrating Neural Networks in the PDR for Hardware Model Checking	2023
Guangyu Hu, Wei Zhang, Hongce Zhang	MLCAD

WORK EXPERIENCE

Senior Research Engineer | *Fermat Lab*

🌸 Huawei Hong Kong Research Center

Dec. 2025 – Present
Hong Kong, China

- Built LLM reasoning pipelines for formal proof refereeing, converting natural-language and vision-model proof traces into geometry predicates and verifiable subgoals.
- Implemented subgoal-to-predicate conversion components with constrained decoding, predicate validation, fine-tuning experiments, and iterative subgoal promotion on Newclid-based proofs.
- Contributed to FermatVerification, an LLM-agent-driven C program verification toolkit, with agent workflows and Frama-C/ACSL/WP integration for specification and proof automation.
- Contributed to FermatVerification-RTL, a hardware security verifier that checks whether secret data can affect observable RTL signals, using self-composition miters and Yosys/sby backends.

Research Internship | *Noah's Ark Lab*

🌸 Huawei Technologies

Sep. 2024 – Mar. 2025
Shenzhen, China

- Developed a word-level hardware model checker based on Pono with high efficiency.
- Designed an interface that allows verification engineers to insert lemmas, assertions, and clauses using large language models.
- Implemented a circuit-aware solver tuner that automatically selects the optimal configuration based on circuit features.
- Optimized parameter selection for Kissat, eliminating the need for manual tuning.

PROJECT HIGHLIGHTS

EvolveGen

TACAS'26

- (i) Built the **first algorithm-level hardware-model-checking benchmark generator**, coupling reinforcement learning with HLS to produce solver-targeted “small-but-hard” instances.
- (ii) Co-generated and submitted **611 bit-vector benchmarks (611 safety properties)** to [HWMCC'25](#) officially credited by the organizers as a benchmark contributor.

Learning-Guided IC3/ PDR

MLCAD'23, ASP-DAC'24,
CAV'26, ISEDA'26,
DAC'26

- (i) Pioneered advanced ML-guided hardware model checking through five first-of-their-kind, open-source systems: [AutoPDR](#) (circuit-aware solver configuration), [A-IC3](#) (online contextual-bandit generalization), [NeuroPDR](#) (online GNN generalization), [DeepIC3](#) (offline GNN clause prediction), and [LeGend](#) (global-representation lemma generation).
- (ii) Demonstrated **26–50 more solved cases** (A-IC3), **up to 10.8× speed-up** (DeepIC3), **26.4% lower convergence time** (NeuroPDR), and **90% more solved instances** (AutoPDR) while preserving formal soundness.

E-Syn & E-Morphic

DAC'24, DAC'25

- (i) Introduced **equality saturation to gate-level Boolean logic optimization**, then scaled it to post-optimization resynthesis for structural exploration before technology mapping.
- (ii) Improved ABC by **15.29% in delay / 6.42% in area** (E-Syn) and **7.29% in delay / 12.54% in area** on large EPFL circuits (E-Morphic).
- (iii) Open-sourced both frameworks, attracting **50+ citations** and **70+ GitHub stars** within two years.

OPEN-SOURCE CONTRIBUTIONS

🔗 [rIC3](#)

State-of-the-art hardware
model checker

100+ stars, 2 merged PRs

[PR #157](#) – Implemented the MAB-guided IC3 inductive generalization used by [A-IC3](#) (CAV 2026).

[PR #12](#) – Added legacy AIGER compatibility for broader benchmark support.

🔗 [Z3](#)

Widely used SMT solver

12k+ stars, 3 merged PRs

Merged [PR #9245](#), [#9246](#), and [#9303](#) to strengthen Z3's mini-IC3 engine in Python, and resolved correctness issues across the examples. Extended this work into [pyBMC](#), a Z3Py bounded model checker, and [pyIC3](#), a standalone IC3/PDR implementation; both support AIGER 1.0.

SELECTED HONORS AND AWARDS

 **2nd place – Logic and Structure Analysis for Large-scale Digital Circuits** Summer 2025
Xiakedao EDA² Challenge

 **3rd place – Hardware Model Checking Competition** Spring 2024
Xiakedao EDA² Challenge

Full Postgraduate Scholarship Spring 2021 – Spring 2026
The Hong Kong University of Science and Technology

Distinction Award with Third-Class University Scholarship Fall 2019
Xiamen University

TALKS & PRESENTATIONS

Cheetah: A Property-based Parallel BMC Engine Spring 2024
International Symposium of EDA (Xi'an, Shaanxi, China)

Equality Saturation Framework for Next-generation Logic Synthesis Fall 2024
CUHK Bei Yu's Lab (Hong Kong, China)

TEACHING EXPERIENCE

Logic Design Automation of Digital Systems Fall 2022
The Hong Kong University of Science and Technology

Formal Methods and Testing for Electronic System Verification Spring 2023
The Hong Kong University of Science and Technology

RELEVANT COURSEWORK

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- | | |
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| <ul style="list-style-type: none">• GPU Architectures and Programming• Introduction to Graph Learning• Introduction to Formal Methods• Logic Design Automation of Digital Systems• Automated Reasoning in Electronic System Verification | <ul style="list-style-type: none">• C and C++ Programming• Data Structure• Algorithm Analysis and Design• Operating Systems• Database• Fundamentals of Network Technology |
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SKILLS

Languages: English (Proficient), Chinese Mandarin (Native), Cantonese (Native)
Programming: C & C++, Python, Rust, R, Haskell, MATLAB, Java, Julia, CUDA, SQL, Shell scripting
Electronics Design Automation Software: JasperGold, Design Compiler, KiCad, Xilinx Vivado, Yosys, Berkeley ABC, The EPFL Logic Synthesis Libraries (caterpillar, lorina, mockturtle, etc.)
Platforms and Tools: GNU/Linux, KVM/QEMU, Windows/WSL2, Slurm for Linux clusters, CLI (Docker, Git, Vim, etc.), Hadoop Ecosystem (HBase, HDFS, Spark, etc.)
ML & DL Framework: PyTorch, Scikit-learn, TensorFlow, Keras, PySpark, mlpack, PyG, DGL
Document Creation: Microsoft Office Suite, LaTeX, Markdown

SERVICE

Technical Programme Committee
VMCAI 2027, ISEDA 2026

Sub-Reviewer & Student Reviewer
DAC 2026, ASPDAC 2025, FMCAD 2024

Artifact Evaluation Committee
CAV 2025, TACAS 2025, OOPSLA 2025, FAST 2024, iFM 2024 2025
HWMCC2024, HWMCC2025 Benchmark Contributor
github.com/Gy-Hu/HWMCC24-benchmark